TDC3310

Video D/A Converter

10-Bit, 40 Msps

Features

- 10-bit resolution
- Single +5 volt power supply operation
- DC to 40 Msps, guaranteed
- ±1.0 LSB linearity error
- TTL-compatible inputs
- 1 Vp-p video output
- Sync and Blank controls
- Video invert control
- Very low glitch energy
- Very low cost

Applications

- Reconstruction of composite video
- High-resolution video
- Low-cost video systems
- Set-top RF converter boxes
- Satellite receivers
- Direct digital synthesis
- Multimedia

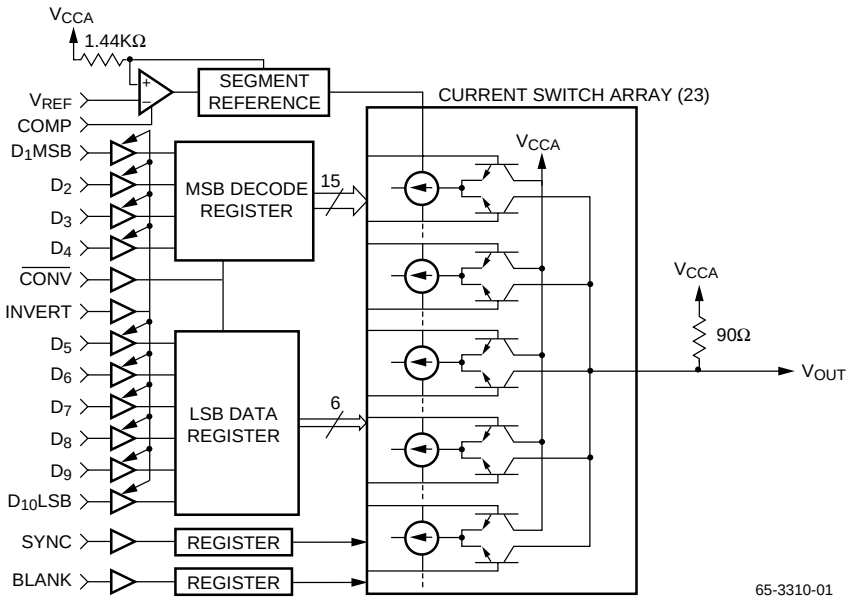
Description

The TDC3310 is a very high-speed 10-bit D/A converter especially suited for low-cost video applications. The TDC3310 offers 10-bit resolution, TTL-compatible inputs, and requires only a single +5 volt power supply. It has a single-ended voltage output, SYNC and BLANKing control inputs and an INVERT input that reverses video levels without altering either SYNC or BLANKing.

Operating at data rates up to 40 Msps, the TDC3310 is ideal for reconstructing composite NTSC, PAL and RS-343A video waveforms. Data is decoded and registered ahead of the current switch array, resulting in outstanding low-glitch characteristics.

The TDC3310 is available in a 32-Lead Plastic J-Leaded PLCC and 28-pin plastic packages and is guaranteed from 0°C to 70°C.

Block Diagram



Functional Description

The TDC3310 consists of five major circuit sections: the data and control registers, the MSB decode block, the MSB current switch array, the binary weighted LSB array and the reference amplifier. All inputs are registered just before the current switch array to minimize the temporal skew that generates glitches.

The TDC3310 uses an architecture that combines segmentation and binary weighted techniques. With the four MSBs segmented into 15 equal-value current switches, and the six LSBs using binary weighting, an optimal trade-off between glitch performance and die size (cost to the user) is made. The result is a very low cost, high performance D/A converter.

Power and Ground

The TDC3310 requires a single +5.0 volt power supply. The analog (V_{CCA}) and digital (V_{CCD}) power supply voltages should be separately decoupled, as shown in Figure 8, to reduce power supply induced noise. 0.1 µF decoupling capacitors should be placed as close as possible to the TDC3310 power pins. Ferrite beads are neither critical in value nor always required.

The high slew rate of digital data makes capacitive coupling to the outputs of any D/A converter a potential problem. Since the digital signals contain high frequency harmonics of the $\overline{CONV}$ signal, as well as the video output signal, the result of data feedthrough often looks like harmonic distortion or reduced signal-to-noise performance, Separate analog and digital grounds are provided on the TDC3310, but all ground pins should be connected to a common solid ground plane for best performance.

V_{REF}

The TDC3310 is designed to operate with a voltage reference referred to V_{CCA} (a 1V difference between V_{REF} and V_{CCA}). The TDC3310 uses this voltage differential to generate an internal reference current for the current switch array. Since the DC voltage provided to V_{REF} must be referred to V_{CCA} (and not A_{GND}), the output voltage of the D/A converter is referred toV_{CCA} (and not to A_{GND}). This allows the gain of the TDC3310 to be immune from variations of V_{CCA}. V_{REF} should be decoupled to V_{CCA}.

The internal reference amplifier has a high-impedance input and is externally frequency-compensated to ensure stability. A 0.1 µF capacitor should be connected between the COMP pin and A_{GND}. The Typical Interface Circuits, shown in Figure 8, include an adjustable reference circuit.

Data Inputs $D_{1\text{-}10}$

The data inputs are TTL-compatible. For applications involving fewer than 10 bits, connect the unused LSBs to D_{GND}.

$\overline{CONV}$

The TDC3310 requires a TTL-compatible clock signal, $\overline{CONV}$. All inputs are registered on and the analog output changes t_{CO} after the falling edge of $\overline{CONV}$.

SYNC and BLANK

SYNC and BLANK inputs control the output level of the TDC3310 during CRT retrace intervals. When BLANK is HIGH, data to $D_{1\text{-}10}$ are ignored and V_{OUT} is forced to a fixed blanking level, nominally 81 mV below the video "black" level. When SYNC is HIGH, data to $D_{1\text{-}10}$ and BLANK are ignored and V_{OUT} is forced to a fixed sync level, nominally 433mV below the level corresponding to BLANK. SYNC and BLANK are registered within the TDC3310 on the falling edge of $\overline{CONV}$.

INVERT

INVERT controls the polarity of $D_{1\text{-}10}$ without affecting the SYNC or BLANK inputs. This input functions as a system data format selector, allowing the reversal of black and white in a video image. See the Input Coding Table. INVERT is registered within the TDC3310 on the falling edge of $\overline{CONV}$.

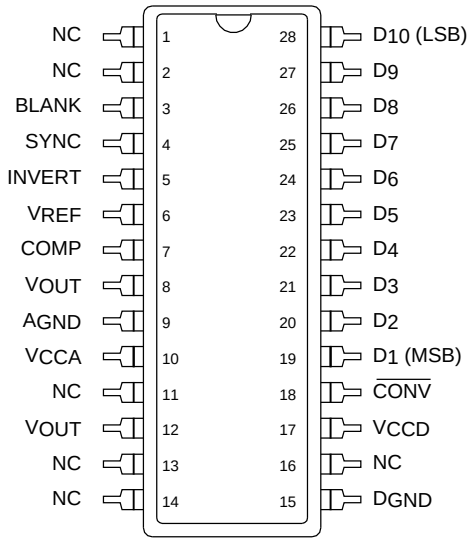
V_{OUT}

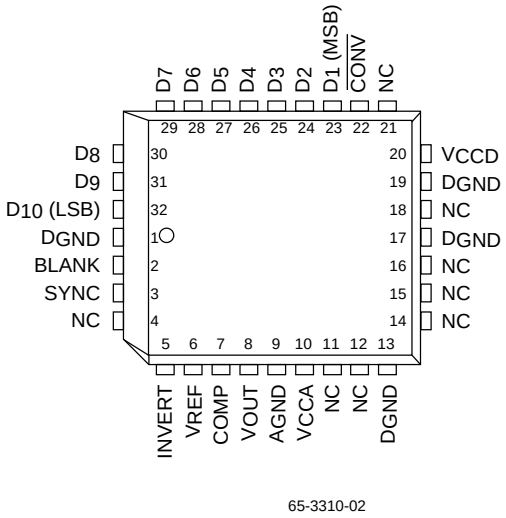
The voltage output of the TDC3310 is referred to V_{CCA} and varies from V_{CCA} to V_{CCA}–V_{REF}. The V_{OUT} terminal of the TDC3310 has an internal 90Ω resistor to provide a voltage output from the current switch array. The close thermal coupling and matched temperature coefficients of the internal reference current generator and this V_{OUT} load resistor provide an output that is stable over temperature. Operation with an external load resistor will reduce output voltage range as well as temperature stability. Current may be driven into or out of the V_{OUT} terminal as long as the output compliance voltage limit of the TDC3310 is not violated.

Not Connected

There are several pins with no internal connection to the TDC3310. They should be left open.

Pin Assignments





65-3310-02

Pin Descriptions

Pin Name	Pin Number PDIP	Pin Number PLCC	Value	Pin Function Description
Power				
V_{CCA}	10	10	5.0V	Analog supply voltage.
V_{CCD}	17	20	5.0V	Digital supply voltage.
Ground				
AGND	9	9	0.0V	Analog ground.
DGND	12, 15	1, 13, 17, 19	0.0V	Digital ground.
Reference				
V_{REF}	6	6	V_{CCA}–1	Reference voltage input.
COMP	7	7	0.1µF	Compensation capacitor.
Data Input				
D_1 (MSB)	19	23	TTL	Most Significant Bit Input.
D_2–D_9	20–27	24–31	TTL	
D_{10} (LSB)	28	32	TTL	Least Significant Bit Input.
INVERT	5	5	TTL	Invert D_1–D_{10}.
SYNC	4	3	TTL	SYNC input.
BLANK	3	2	TTL	BLANK input.
Clock				
$\overline{CONV}$	18	22	TTL	Clock input.
Output				
V_{OUT}	8	8	+4 to +5	Analog output.
No Connect				
NC	1, 2, 11, 13, 14, 16	4, 11, 12, 14–16, 18, 21	Open	Not connected.

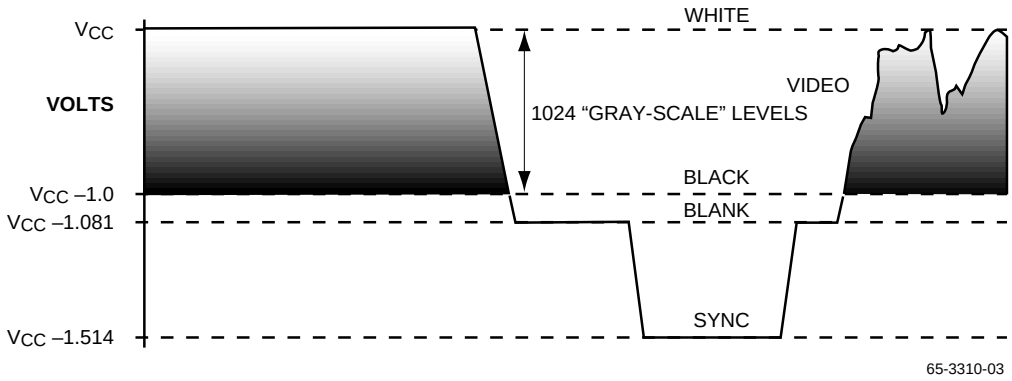


Figure 1. Video Output Waveforms

Absolute Maximum Ratings[1]

Type	Parameter	Min.	Max.	Unit
Supply Voltages	V_{CCA} (measured to A_{GND})	-0.5	+7.0	V
	V_{CCD} (measured to D_{GND})	-0.5	+7.0	V
	V_{CCA} (measured to V_{CCD})	-0.5	+0.5	V
	A_{GND} (measured to D_{GND})	-0.5	+0.5	V
Inputs	$\overline{CONV}$, $D_{1–10}$, SYNC, BLANK, INVERT			
	Applied voltage (measured to D_{GND})[2]	-0 5	+7.0	V
	Externally forced current[3]	–10	+10	mA
	V_{REF}			
	Applied voltage (measured to A_{GND})[2]	-0 5	V_{CCA} + 2	V
	Externally forced current[3]	-10	+10	mA
Output	V_{OUT}			
	Applied voltage (measured to A_{GND})[2]	+3.0	7.0	V
	Externally forced current[3]	-20	+20	mA
Temperature	R6 Package			
	Operating, ambient	-25	+90	°C
	Junction		+140	°C
	B6 Package			
	Operating, ambient	-60	+150	°C
	Junction		+200	°C
	Lead, soldering (10 seconds)		+300	°C
	Storage	-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied to individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Device performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.

Operating Conditions

Parameter	Description	Min.	Nom.	Max.	Unit
V_{CCA}	Analog Power Supply Voltage	4.75	5.00	5.25	V
V_{DDC}	Digital Power Supply Voltage	4.75	5.00	5.25	V
V_{CCA}–V_{CCD}	Power Supply Voltage Differential	-0.1	0.0	0.1	V
A_{GND}–D_{GND}	Ground Voltage Differential	-0.1	0.0	0.1	V
V_{REF}	Reference Voltage	V_{CCA}–1.5	V_{CCA}–1.0	V_{CCA}–0.5	V
C_C	Compensation Capacitor	0.01	0.1		µF
V_{IL}	Input Voltage, Logic LOW			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			V
t_S	Input Data Setup Time	20			ns
t_H	Input Data Hold Time	2			ns
t_{PWL}	$\overline{CONV}$ Pulse Width, LOW	10			ns
t_{PWH}	$\overline{CONV}$ Pulse Width, HIGH	10			ns
T_A	Temperature Range, Still Air	0		70	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	V_{CCD} = V_{CCA} = Maximum		70	115	mA
C_{IN}	Input Capacitance	$\overline{CONV}$, $D_{1\text{-}10}$, SYNC, BLANK, INVERT, V_{REF}		5	10	pF
I_{IL}	Input Current, Logic LOW	V_{CCD} = Max., V_I = 0.4V		-200	-400	µA
I_{IH}	Input Current, Logic HIGH	V_{DDC} = Max., V_I = 2.4V		10	100	pA
R_O	Output Resistance	V_{OUT} to V_{CCA}, T_A = +25°C	80	90	100	Ω
C_O	Output Capacitance	V_{OUT} Terminal			20	pF
V_{OC}	Output Compliance	Referred to V_{CCA}	-1.5	0	+0.4	V
V_{FS}	Full-Scale Output	Referred to V_{CCA}, V_{REF} = Nominal	-0.95	-1.0	-1.05	V
V_{BLANK}	Blank Output Voltage	Referred to V_{FS}, V_{REF} = Nominal	-71	-81	-91	mV
V_{SYNC}	Sync Output Voltage	Referred to V_{BLANK}, V_{REF} = Nominal	-380	-433	-480	mV

AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_S	Maximum Clock Rate	V_{CCA}, V_{CCD} = Minimum	40			MHz
t_{CO}	Clock to Output Delay[1, 2]	V_{CCA}, V_{DDC} = Minimum		8	15	ns
t_R	Output Risetime[1, 2]	90% to 10% of Full Scale		5	10	ns
t_F	Output Falltime[1, 2]	10 to 90% of Full Scale		5	10	ns
t_{SET}	Output Settling Time[1, 2, 3]	to 1%		10	18	ns
		to +1 LSB		25	40	ns
G_A	Peak Glitch Area[2,3]			50		pV-sec

Notes:

1. See Timing Diagram.
2. Standard Test Load, Figure 4.
3. Worst-case transition.

System Performance Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E_{LD}	Differential Linearity Error	V_{CCA}, V_{CCD}, V_{REF} = Nom.		±0.5	±1.0	LSB
E_{LI}	Integral Linearity Error	V_{CCA}, V_{CCD}, V_{REF} = Nom..		±0.5	±1.0	LSB
E_G	Absolute Gain Error	V_{CCA}, V_{CCD}, V_{REF} = Nom.		±1	±5	%
T_{CEG}	Gain Error Tempco	V_{CCA}, V_{CCD}, V_{REF} = Nom.		±30		ppm/°C
V_{OF}	Output Offset Voltage	V_{CCA}, V_{CCD} = Max., $D_{1–10}$ = HIGH		-10	-25	mV
T_{COF}	Offset Tempco	V_{CCA}, V_{CCD} = Max., $D_{1–10}$ = HIGH		-50		µV/°C
I_{REF}	V_{REF} Input Bias Current			1	5	µA
D_P	Differential Phase	f_S = 4 x NTSC Subcarrier		0.2		Degrees
D_G	Differential Gain	f_S = 4 x NTSC Subcarrier		0.3		%

Performance Curves

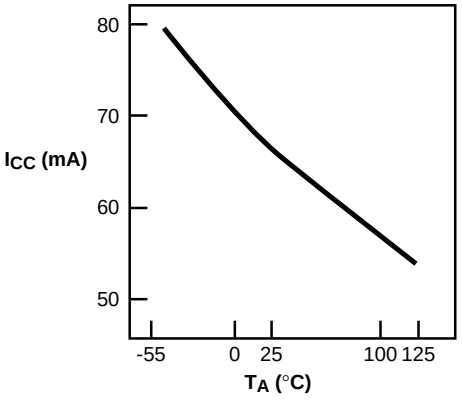


Figure 2. Power Supply vs. Temperature

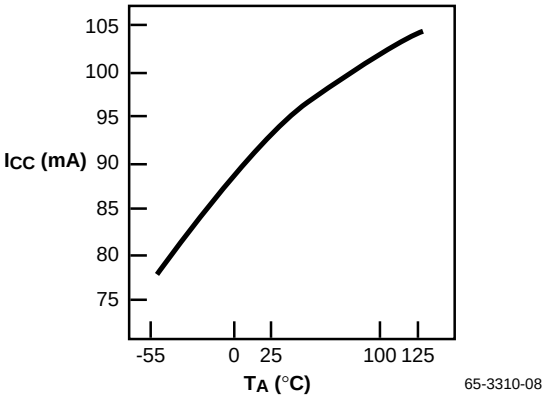


Figure 3. R_{OUT} vs. Temperature

Input Coding Table

D1.....D10 (MSB LSB)	BLANK	SYNC	INVERT = LOW V_{OUT} w/r V_{CCA}	V_{OUT} w/r AGND	INVERT = HIGH V_{OUT} w/r V_{CCA}	V_{OUT} w/r AGND
11 1111 1111	0	0	0.000	5.000	-1.000	4.000
11 1111 1110	0	0	-0.001	4.999	-0.999	4.001
11 1111 1101	0	0	-0.002	4.998	-0.998	4.002
:	:	:	:	:	:	:
10 0000 0000	0	0	-0.500	4.500	-0.501	4.499
01 1111 1111	0	0	-0.501	4.499	-0.500	4.500
:	:	:	:	:	:	:
00 0000 0010	0	0	-0.998	4.002	-0.002	4.998
00 0000 0001	0	0	-0.999	4.001	-0.001	4.999
00 0000 0000	0	0	-1.000	4.000	0.000	5.000
xx xxxx xxxx	1	0	-1.081	3.919	-1.081	3.919
xx xxxx xxxx	x	1	-1.514	3.486	-1.514	3.486

Note:

1. V_{REF} = V_{CCA} – 1.000 volts, V_{CCA} = 5.0 volts, no external.

Timing Diagrams

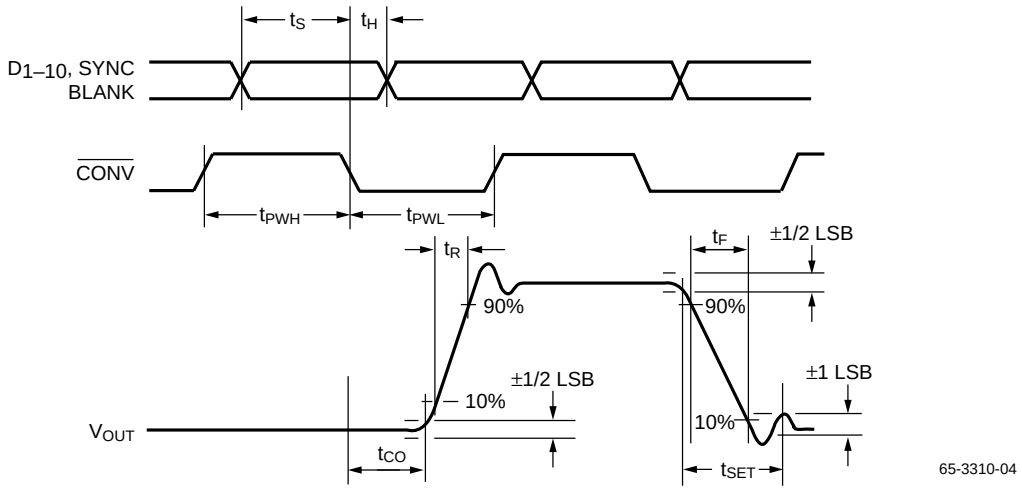


Figure 4. Timing Diagram

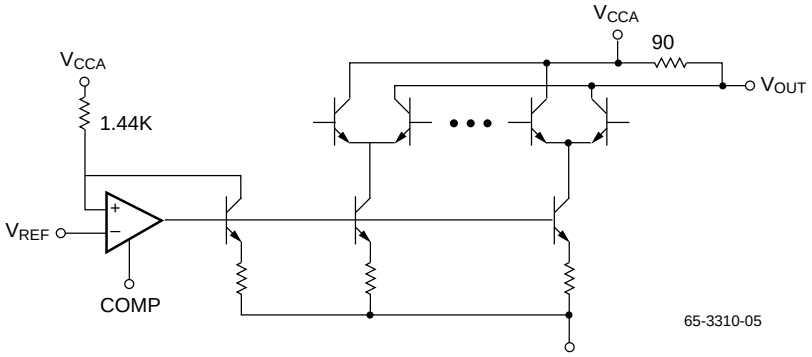


Figure 5. Equivalent Reference and Output Circuit

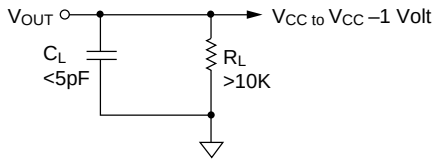


Figure 6. Output Test Load

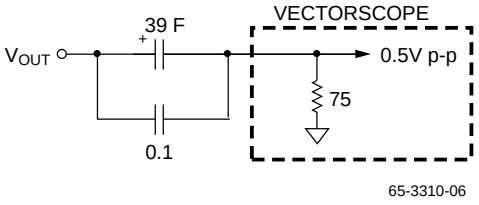


Figure 7. Output Load for DP and DG

Application Notes

Since the internal reference and output circuits of the TDC3310 are referred to the power supply, V_{CC}, the external voltage reference shown in the Typical Interface Circuit is also referred to V_{CC}. A simple 1.2 volt Bandgap reference diode is voltage-divided to provide 1.0 volts between the V_{REF} and V_{CC} inputs. The output of the TDC3310 is AC coupled into a 75Ω resistor which divides the output video level by a factor of two. The video amplifier gain is +2, restoring the 1 Vp-p video level and referring the video signal to A_{GND}. It is important to ensure the power supply for the TDC3310 is well-regulated and free of high-frequency noise. Careful power supply decoupling will ensure the highest quality video signals at the output of the circuit.

Grounding

The TDC3310 has separate analog and digital circuits. To keep digital system noise from the D/A converter, it is recommended that power supply voltages (V_{DDD} and V_{DDA}) come from the same source and ground connections (D_{GND} and A_{GND}) be made to the analog ground plane. Power supply pins should be individually decoupled at the pin.

The digital circuitry that gets its input from the TMC1173 should be referred on the system digital ground plane.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Wire-wrap is not an option—even for breadboarding. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions when doing the layout.

1. Keep the critical analog traces (V_{IN}, R_T, R_B, V_{R+}, V_{R-}) as short as possible and as far as possible away from all digital signals. The TMC1173 should be located near the board edge, close to the analog output connectors.

2. The power plane for the TMC1173 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC1173 is the same as that of the system's digital circuitry, power to the TMC1173 should be decoupled with ferrite beads and 0.1 µF capacitors to reduce noise.

3. The ground plane should be solid, not crosshatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They typically supply adjacent circuitry on the device, which generate varying amounts of noise. For best results, use 0.1 µF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not overlap the TMC1173, the voltage reference or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC1173 and its related analog circuitry can have an adverse effect on performance.

6. $\overline{CONV}$ should be handled carefully. Jitter and noise on this clock may degrade performance. Terminate the clock line carefully to eliminate overshoot and ringing.

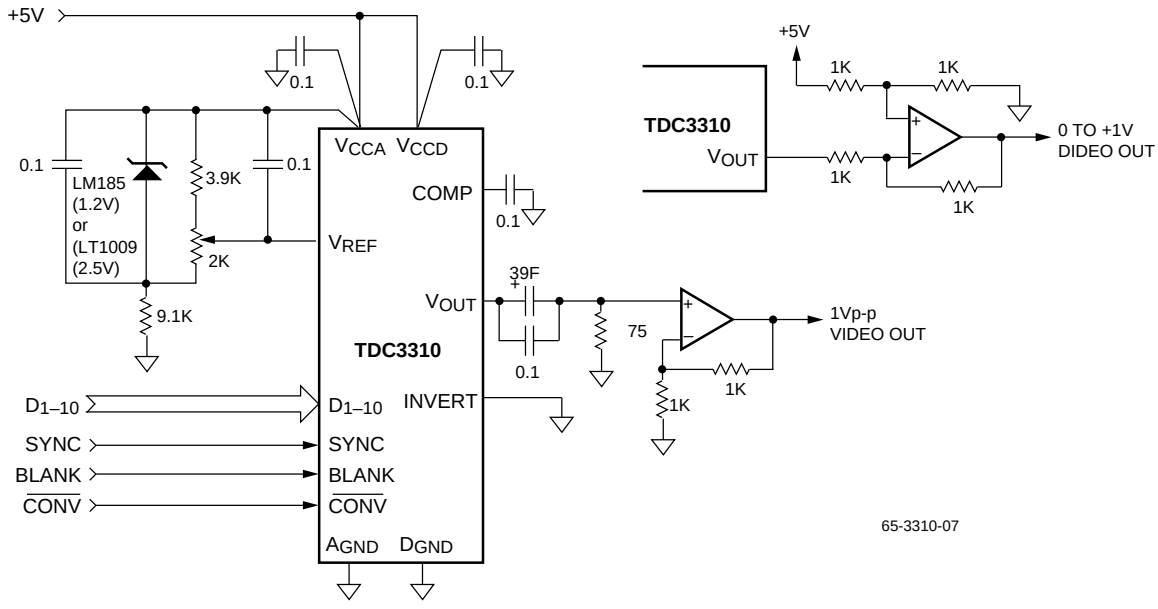


Figure 8. Typical Interface Circuit

Notes:

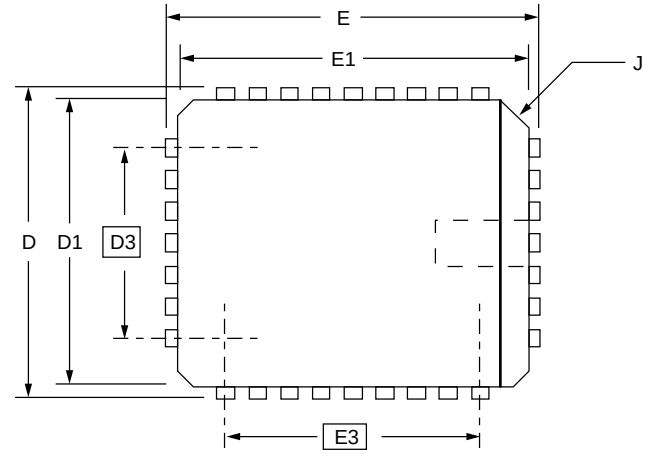
Mechanical Dimensions

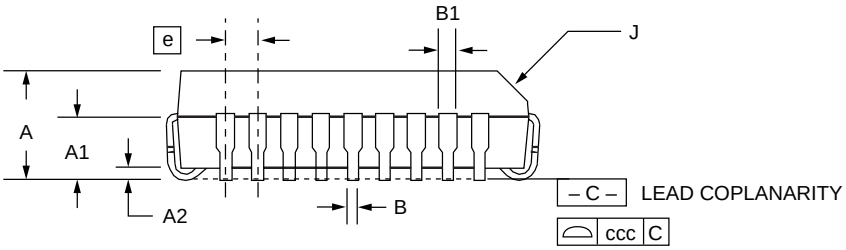
32 Lead Plastic Chip Carrier

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.126	.146	3.20	3.71	
A1	.054	.074	1.37	1.88	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D	.480	.500	12.19	12.70	
E	.580	.600	14.73	15.24	
D1	.438	.458	11.12	11.63	3
E1	.538	.558	13.67	14.17	3
D3	.300 BSC		7.62 BSC		
E3	.500 BSC		12.70 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	7/9		7/9		
N	32		32		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101 inch (.245mm)





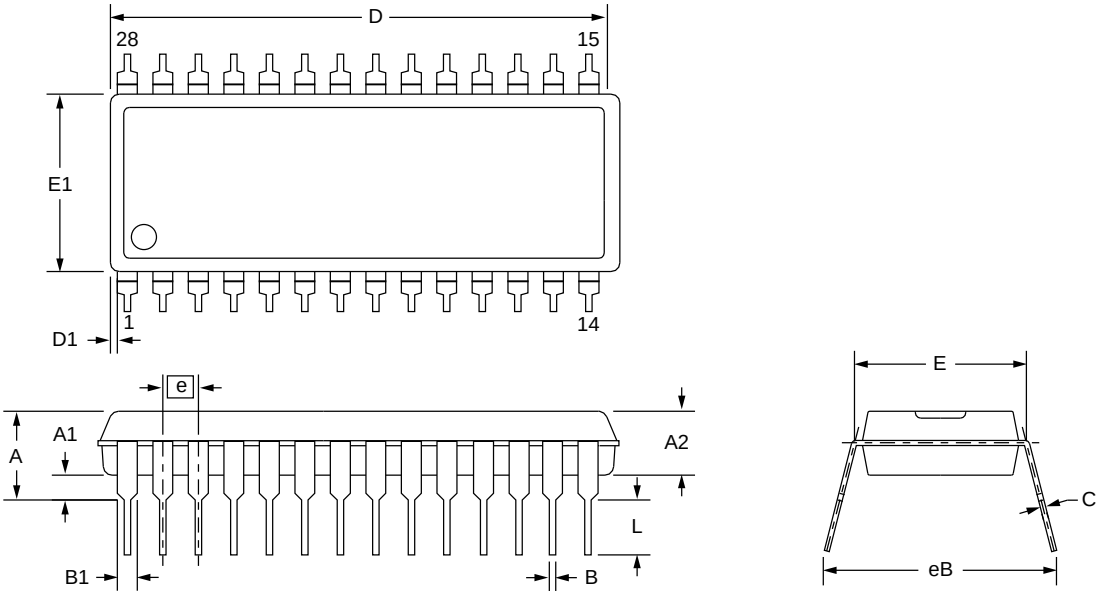
Mechanical Dimensions (continued)

28 Lead Plastic DIP – .600" Body Width

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.250	—	6.35	
A1	.015	—	.38	—	
A2	.125	.195	3.18	4.95	
B	.014	.022	.36	.56	
B1	.030	.070	.76	1.78	
C	.008	.015	.20	.38	4
D	1.380	1.565	35.05	39.75	2
D1	.005	—	.13	—	
E	.600	.625	15.24	15.88	
E1	.485	.580	12.32	14.73	2
e	.100 BSC		2.54 BSC		
eB	—	.700	—	17.78	
L	.115	.200	2.92	5.08	
N	28		28		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are shown for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Linearity Error (LSB)	Temperature Range	Screening	Package	Package Marking
TDC3310N6C	±1.0	T_A = 0°C to 70°C	Commercial	28-pin Plastic DIP	3310N6C
TDC3310R6C	±1.0	T_A = 0°C to 70°C	Commercial	32-Lead J-Lead PLCC	3310R6C
TMC1175E1C	30	T_A = 0°C to 70°C	Commercial	Eurocard PC Board	TMC1175E1C

Raytheon Electronics
Semiconductor Division
5580 Morehouse Drive
San Diego, CA 92121
619 457 1000
800 722 7074
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applications@lj.sd.ray.com

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